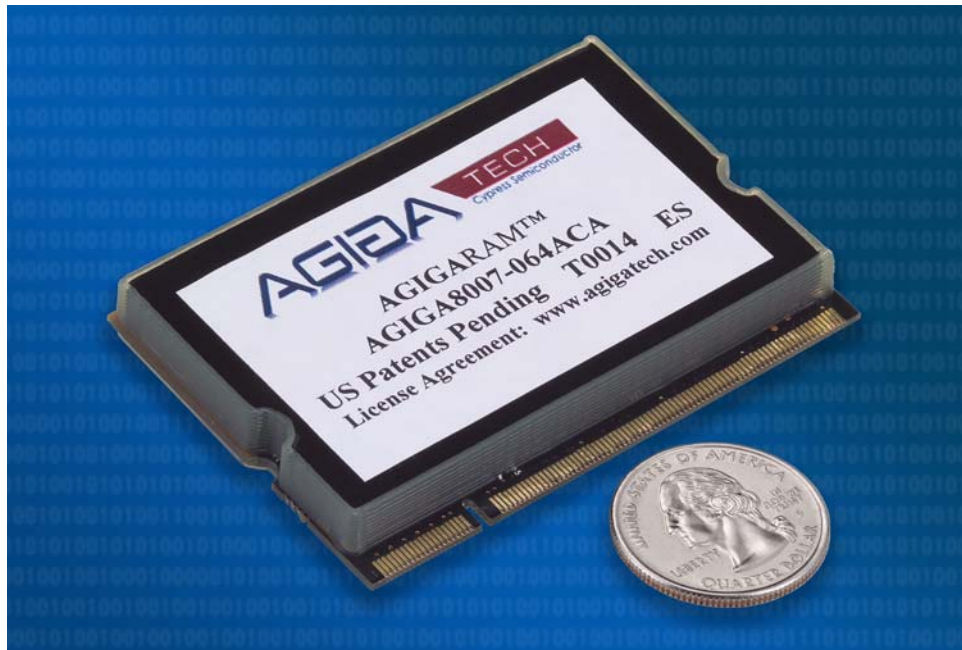


Product Specification

Bali Non-Volatile System



The **AGIGARAM™** Bali Non-Volatile System is an easy-to-use module for industrial controls, medical equipment, gaming systems, and other embedded applications that require large amounts of fast, non-volatile memory. This system is offered in the following configurations:

Ordering Information

Device P/N	Density		Organization	Vcc
	Total	Non-Volatile		
AGIGA8003-004ACA	32 MBytes	4 MBytes	16M x 16	3.3V
AGIGA8004-008ACA	32 MBytes	8 MBytes	16M x 16	3.3V
AGIGA8005-016ACA	32 MBytes	16 MBytes	16M x 16	3.3V
AGIGA8006-032ACA	32 MBytes	32 MBytes	16M x 16	3.3V
AGIGA8007-064ACA	64 MBytes	64 MBytes	32M x 16	5.0V*

*SDRAM and control signal interfaces are 3.3V.

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Revision History

Revision	Date	Description of Changes
P/N 001-8000-00, Rev A	March 2009	Initial release.
P/N 001-8000-00, Rev B	April 2009	Updated to add information about I ² C and LED indicators.
P/N 001-8000-00, Rev C	May 2009	Corrected P/Ns, corrected Pin 143 in pin diagram, added LED illustration, and updated threshold values.
P/N 001-8000-00, Rev D	June 2009	Ch 2: Added pin type ODPUs (Open-drain with weak pull-up) and updated tables. Ch 3: Added DC specifications for Bali control signals.

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Introduction

In response to the needs of customers for a fundamentally better approach to implementing large high-speed, non-volatile RAM, AGIGATech presents the **AGIGARAM™** Bali Non-Volatile System (NVS). This system provides a high-density, battery-free, non-volatile memory solution in a compact package.

1.1 Product Overview

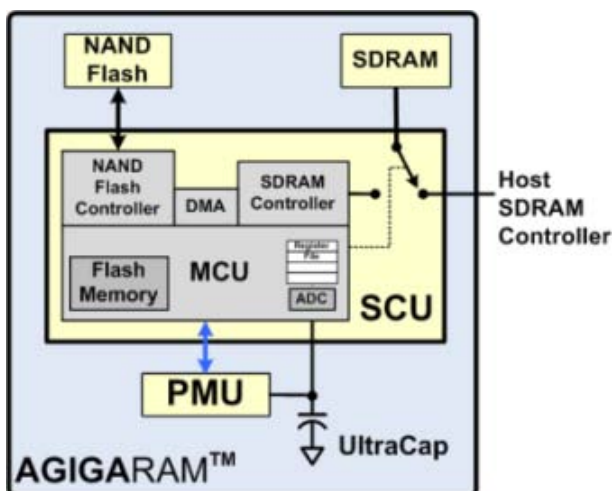
The **AGIGARAM** Bali Non-Volatile System (referred to as Bali in the remainder of this document) delivers the highest capacity non-volatile RAM available in the industry. Available in SDRAM sizes of 32MB and 64MB, with non-volatile portions ranging from 4MB to 64MB, Bali offers interfaces that provide fast time-to-market and high performance.

Traditional approaches have made nvRAMs greater than 4 to 8 Megabits impractical due to technology limitations, cost, and lack of a convenient power source. As a result, nvRAM has been limited to specialty applications or those with workarounds for issues from power sources (such as batteries).

Now, Bali provides a high-density, battery-free, non-volatile solution. This NVS delivers unlimited read/write performance at RAM speeds, while also safely backing up SDRAM data when power is interrupted. The system provides the dual advantages of fast, non-wear random access plus non-volatility. In addition, Bali brings a whole new set of system-level features and reliability to the designer.

The Bali Non-Volatile System is an easy-to-use, turnkey system that can enable many value-added system features. These features include zero standby, power interruption immunity, rapid on/recovery, write caching/posting, data logging, service/maintenance processing, journaling, unified memory architectures, and UPS replacement/redundancy—all while preserving mission-critical data.

[Figure 1-1](#) shows the system-level block diagram for the Bali Non-Volatile System.



SCU=System Control Unit, PMU=Power Management Unit

Figure 1-1 Bali System Block Diagram

This system delivers unlimited Read/Write capability at RAM speeds, while also safely backing up SDRAM data when power is interrupted. This system approach utilizes the best features of proven memory technologies—fast, non-wear random access plus non-volatility. The system controller also monitors and manages a battery-free power source to optimize system performance.

Bali may be powered by a single 3.3v or 5.0v supply. This power management circuitry provides regulated power to internal Bali components. Upon power interruption, this circuitry is powered by the on-board power source, ensuring continuity of power while the contents of the memory are saved. When the Save operation is completed, Bali can shut down with no requirement for back-up power.

1.2 Features

Bali offers the following features:

- The highest capacity non-volatile RAM available
- A complete, integrated Non-Volatile System (NVS)
 - High reliability
 - Small board area requirement (high density; MB/area)
 - Enables fast time-to-market
 - Lower cost of ownership
 - Easy to use
- Looks like an SDRAM to a Host system, with non-volatility completely managed by Bali
 - Unlimited read/write cycles
 - No wear issues
 - I²C interface available
- Simple high speed standard SDRAM interface, plus four added control signals:
 - Host initiates an SDRAM-to-Flash Save operation
 - Bali indicates System Ready
 - Host initiates an SDRAM Flash Restore operation
 - Bali indicates Vcc Drop and automatically starts an SDRAM-to-Flash Save operation
- Variable partitioning: user specified volatile and non-volatile memory sizes
 - Host system can specify size all or portion of RAM size to be non-volatile
 - System configurable via I²C
- Battery-free internal power source
 - Powers the Bali Non-Volatile System when the Host loses power
 - 5-year and 10-year operating life available
 - 10-year data retention
 - Minimum 200,000 power cycles
 - Continuous health monitoring
 - No catastrophic failure modes
 - High temperature operation (10 years @ 40°C, 5 years @ 70°C)
- Automatic history tracking: Tracks critical internal system parameters
- Intelligent Fast Recovery
 - Fast start/recovery on short power interruptions

- **AGIGASAFE™** Archival Image Protection
 - Bali can keep a snapshot of the RAM contents
 - Useful in retaining factory default settings, clean OS images, and other mission-critical data
- System Safe: Interlocking control sequence for safe operation
- Standard low-cost 200-pin connector

Note

Although the Bali package fits into the same connector as a 200-pin SOIMM memory card, Bali is **not** pin-compatible with SDRAM modules that use this connector.

Single supply

- RoHS-compliant, battery-free, no hazardous material issues
- Comprehensive support available
 - Demo board
 - A complete suite of product documentation, including
 - Product Brief
 - Datasheet (this Product Specification)
 - Technology White Paper
 - Application Notes and Technical Notes

Pin Layout and Descriptions

This chapter describes the 200-pin package for the **AGIGARAM™** Bali Non-Volatile System.

2.1 Pin Types

[Table 2-1](#) lists the pin functions in this package.

Table 2-1 Pin Types

Pin Type	Description
I	Input
IPD	Input with weak pull-down
IO	Bidirectional
OD	Open-drain output
PWR	Power
GND	Ground
ODPU	Open-drain with weak pull-up

NOTE: Pins marked with a dash (—) in [Figure 2-1](#) designate a “Do Not Connect” pin.

2.2 Pin Layout

[Figure 2-1](#) lists the pin locations.

Bali is available in 5.0V and 3.3V versions. Connect V_{CC} for either version to Pins 9–18.

Pins identified as DNC (—) in [Figure 2-1](#) are Reserved and must **not** be connected.

Note

Although the Bali connector is the same as a 200-pin DIMM, the Bali package is **not** compatible with SDRAM modules that use this connector.

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	GND	2	GND	69	—	70	—	137	—	138	—
3	GND	4	GND	71	—	72	—	139	FORCE_SAVE	140	—
5	GND	6	GND	73	—	74	—	141	FORCE_RESTORE	142	CS#
7	—	8	—	75	—	76	—	143	ARCHIVE	144	WE#
9	VCC	10	VCC	77	—	78	—	145	POWER_FAIL_INT#	146	RAS#
11	VCC	12	VCC	79	—	80	—	147	—	148	CAS#
13	VCC	14	VCC	81	GND	82	GND	149	—	150	DQMU
15	VCC	16	VCC	83	GND	84	GND	151	—	152	DQML
17	VCC	18	VCC	85	GND	86	GND	153	—	154	CKE
19	—	20	—	87	—	88	SCL	155	—	156	CLK
21	GND	22	GND	89	—	90	SDA	157	GND	158	GND
23	GND	24	GND	91	—	92	—	159	GND	160	GND
25	GND	26	GND	93	—	94	—	161	GND	162	GND
27	GND	28	GND	95	—	96	—	163	DQ15	164	BA1
29	GND	30	GND	97	—	98	—	165	DQ14	166	BA0
31	—	32	—	99	—	100	—	167	DQ13	168	—
33	—	34	—	101	—	102	—	169	DQ12	170	A12
35	—	36	—	103	—	104	—	171	DQ11	172	A11
37	—	38	—	105	—	106	—	173	DQ10	174	A10
39	—	40	—	107	—	108	—	175	DQ9	176	A9
41	GND	42	GND	109	—	110	—	177	DQ8	178	A8
43	GND	44	GND	111	—	112	—	179	DQ7	180	A7
45	GND	46	GND	113	—	114	—	181	DQ6	182	A6
47	—	48	—	115	—	116	—	183	DQ5	184	A5
49	—	50	—	117	—	118	—	185	DQ4	186	A4
51	—	52	—	119	GND	120	GND	187	DQ3	188	A3
53	—	54	—	121	GND	122	GND	189	DQ2	190	A2
55	—	56	—	123	GND	124	GND	191	DQ1	192	A1
57	—	58	—	125	—	126	—	193	DQ0	194	A0
59	—	60	—	127	SYSTEM_READY	128	—	195	GND	196	GND
61	—	62	—	129	—	130	—	197	GND	198	GND
63	—	64	—	131	—	132	—	199	GND	200	GND
65	—	66	—	133	—	134	—				
67	—	68	—	135	—	136	—				

Figure 2-1 Bali Pin Layout

NOTE: Pins marked with a dash (—) designate a DNC (Do Not Connect) pin.

2.3 Pin Descriptions

This section describes pins available for use in the Bali parts, including those for:

- Standard SDRAM signals
- Power signals
- Control signals

2.3.1 SDRAM Signal Pins

[Table 2-2](#) provides SDRAM interface signals. For detailed functional descriptions of these pins and full SDRAM operational details, refer to the appropriate SDRAM datasheet (identified in [Figure 2-5](#)).

Table 2-2 SDRAM Signals

Pin(s)	Name	Type	Description
CLK	System clock	I	Clock to SDRAM and system controller.
CS#	Chip select	I	This signal is passed directly to the Bali SDRAM. If Bali is the only SDRAM in the system, ground this input. If the Host controller supports multiple SDRAMs, connect this pin to one of its Chip Select outputs.
CKE	Clock enable	I	SDRAM clock disabled when CKE=0. The Host should put the SDRAM into the self-refresh mode (CKE=0) before starting a Save operation.
DQ0 ~ DQ15	Data input/output	IO	SDRAM data bus.
A0~A12	Address	I	SDRAM Row/column addresses. <ul style="list-style-type: none"> • 32MB: Row address: RA0~RA12, Column address:CA0~CA8 • 64MB: Row address: RA0~RA12, Column address:CA0~CA9
BA0~BA1	Bank select address	I	SDRAM bank select.
WE#	Write enable	I	Command Inputs. Along with CS#, the pins WE#, RAS#, and CAS# define the SDRAM command being entered.
RAS#	Row address strobe		
CAS#	Column address strobe		
DQML	Data input/output mask	I	SDRAM Input/Output masks.
DQMU	Data input/output mask		

2.3.2 Power and Ground Pins

[Table 2-3](#) provides descriptions for Power and Ground pins.

Table 2-3 Power and Ground Pins

Pin(s)	Name	Type	Description
VCC	3.3V Power supply	I	Supply power to Bali (3.3V±10%).
	5.0V Power supply	I	Supply power to Bali (5.0V±10%).
GND	Power supply	GND	Ground.

2.3.3 Control Signal Pins

In addition to the standard SDRAM control signals, Bali provides seven control pins. [Table 2-4](#) provides detailed pin descriptions.

Table 2-4 Control Signal Pins

Pin(s)	Name	Type	Description
POWER_FAIL_INT#	Power fail detect interrupt	ODPU	Active low, open-drain output with weak pull-up (typ 10K Ω). Bali drives this signal low when Vcc drops below the V _{SAVE} threshold, and floats it (high) when Vcc is above V _{SAVE} . Bali disconnects the SDRAM from the Host at the time t _{DISCON} after asserting the POWER_FAIL_INT# signal.
SYSTEM_READY	Bali SDRAM is available for Host access	ODPU	Active high, open-drain output with weak pull-up (typ 10K Ω). <ul style="list-style-type: none"> LO: The Bali module has control of the SDRAM (not available to Host). The Bali module takes control of the SDRAM under two circumstances: <ol style="list-style-type: none"> During a back-up operation. Bali transfers the SDRAM contents to internal NAND Flash (NF) memory. During a Restore operation. Bali transfers the NAND Flash (NF) contents back to SDRAM. HI: Floats when Host can access SDRAM. The SYSTEM_READY signal goes low at the start of these operations, and floats (high) at completion.
FORCE_SAVE	Host commands a Save operation.	IPD	Active-high input with weak pull-down. The Host can initiate an SDRAM-to-Flash Save operation as long as V _{CC} > V _{SAVE} . The SDRAM Host asserts this signal to start an SDRAM-to-Flash Save operation. SYSTEM_READY drives low when the Save operation starts, and high when it is complete. The Host should assert the FORCE_SAVE signal only after preparing the SDRAM for the Save operation.
FORCE_RESTORE	Host commands a Restore operation	IPD	Active-high input with weak pull-down. Host can initiate a Flash-to-SDRAM Restore operation while V _{CC} > V _{SAVE} . The Host can force a Flash-to-SDRAM Restore operation by asserting this signal. This operation should be performed only when system power is available during the Restore operation.
ARCHIVE	Save/Restore to the protected area	IPD	Active-high input with weak pull-down. The SDRAM Host may assert this signal along with the FORCE_SAVE or FORCE_RESTORE signal to save and restore SDRAM data to a protected area. This protected area is not used during normal Save (as a result of failing power) or Restore operations. This feature may be used to take a “snapshot” of the current SDRAM contents for restoration at a later time. The ARCHIVE signal should be used only when system power (Vcc) is good.
SCL	I ² C slave clock	I	Input. This pin must be pulled up by the Host. I ² C interface clock.
SDA	I ² C slave data	IO	Open-drain, bidirectional. This pin must be pulled up by the Host. I ² C data.

2.4 Host Coordination Using Bali Control Signals

A non-volatile memory system requires coordination between the Host and memory. For example, steps must be taken to ensure that a memory write operation is not in progress when power suddenly fails, so the memory contents are not corrupted.

Bali ensures coordination if the Host meets the following requirements:

1. The Host must have early warning that power is failing, allowing it to institute an orderly shutdown.
2. The Host must put memory into a safe state before handing it off to the Bali system. The safe SDRAM state is its Self-Refresh mode. In this mode, the Clock Enable (CKE) signal is low and all SDRAM control signals except CKE are “don’t care”. The SDRAM refreshes itself in this mode, preserving its contents as the Host-to-Bali switch (and back) is made.

Bali provides functionality using the following signals:

- POWER_FAIL_INT#
- SYSTEM_READY
- FORCE_SAVE
- FORCE_RESTORE
- ARCHIVE

Each signal is described in the following sections.

2.4.1 POWER_FAIL_INT#

Bali drives the POWER_FAIL_INT# signal low when an internal Bali comparator detects Vcc falling below the data-save threshold voltage V_{SAVE} . One millisecond (t_{DISCON}) after driving POWER_FAIL_INT# low, Bali disconnects the SDRAM from the Host interface and begins a Save operation using its local power.

Within one millisecond after POWER_FAIL_INT# asserts, the Host should perform two SDRAM operations in the following order:

1. Program the SDRAM for CL=2 and BL=1, 2, or 4 if not already operating with these parameters [Note: CL=CAS Latency, BL=Burst Length].
2. Put the SDRAM into the self-refresh mode.

The POWER_FAIL_INT# signal is open-drain, active low with an internal pull-up resistor to Vcc. If multiple Bali units are used in a system (for example, to implement a wider data bus), the POWER_FAIL_INT# pins may be wire-OR'd with a common pull-up. The first of the POWER_FAIL_INT# signals to assert will drive the signal low.

2.4.2 SYSTEM_READY

The SYSTEM_READY signal indicates that the Bali SDRAM is available for Host use:

- At power-on, SYSTEM_READY drives low as Bali restores the SDRAM contents and charges its internal power source. When the SDRAM is ready for Host use, SYSTEM_READY floats, causing it to go high due to the external pull-up resistor.
- If Bali asserts the POWER_FAIL_INT# signal (indicating $V_{CC} \leq V_{SAVE}$), SYSTEM_READY drives low t_{DISCON} later (typically 1 millisecond) to indicate that an SDRAM Save operation has started, and the Host no longer has control of the SDRAM. At the end of the Save operation, the SYSTEM_READY signal is in an unspecified state until the Host regains power.
- If the Host initiates a FORCE_SAVE or FORCE_RESTORE operation, the SYSTEM_READY signal immediately drives low. When the Save/Restore operation is complete, the SYSTEM_READY signal floats, causing it to go high due to the external pull-up resistor.

SYSTEM_READY is an active-high open-drain output with an internal pull-up resistor to Vcc. If multiple Bali units are used in a system (for example, to implement a 32-bit or 64-bit data bus), the SYSTEM_READY pins may be wire-OR'd with a common pull-up resistor. The last of the SYSTEM_READY signals to go valid will cause the combined signal to assert (high).

Note

When power is applied and Bali is ready to switch the SDRAM to the Host, it leaves the SDRAM in its self-refresh state along with its settings of CL=2, BL=1, 2, or 4. (CL=CAS Latency, BL=Burst Length).

- If the Host does not use these settings, it must re-initialize the SDRAM for its own settings before accessing the SDRAM (a normal occurrence at power-on).
- Also, if the Host uses different settings, it must reprogram the SDRAM for CL=2 and BL=1, 2, or 4 prior to giving SDRAM control to Bali .

This requirement applies regardless of how control is transferred (that is, using POWER_FAIL_INT#, FORCE_SAVE, or FORCE_RESTORE).

2.4.3 FORCE_SAVE

The FORCE_SAVE signal gives a Host an earlier opportunity to start a Save operation based on its own power-fail circuitry. FORCE_SAVE can also be used to save an archival copy of the SDRAM while the Host is powered. Bali recognizes the FORCE_SAVE signal only when power is good; that is, the POWER_FAIL_INT# is not asserted. Bali ignores FORCE_SAVE if the Host asserts it after POWER_FAIL_INT# asserts.

2.4.4 FORCE_RESTORE

The Host can assert FORCE_RESTORE to initiate an SDRAM Restore operation. This signal is normally used to perform an Archive–Restore operation while the Host is powered. Bali recognizes the FORCE_RESTORE signal only when power is good; that is, when POWER_FAIL_INT# is not asserted. Bali ignores FORCE_RESTORE if the Host asserts it after POWER_FAIL_INT# asserts.

2.4.5 ARCHIVE (AGIGASAFE™ Feature)

Bali uses two flash memory spaces, called Normal and Archive, to save and restore SDRAM contents.

- The Normal space is used by default when power is lost or restored (ARCHIVE = 0).
- The Archive area allows the Host to save and restore a “snapshot” of the current SDRAM contents (ARCHIVE = 1).

The ARCHIVE bit must be valid at the time the Host asserts either the FORCE_SAVE or FORCE_RESTORE signal.

Note
At power-on, SDRAM data is always restored from the Normal space, regardless of the state of the ARCHIVE bit. The ARCHIVE bit is intended to be used when the Host is powered, to allow the Host to save and restore SDRAM “snapshots”.

[Figure 2-2](#) illustrates the interaction between these signals and the Save and Restore operations.

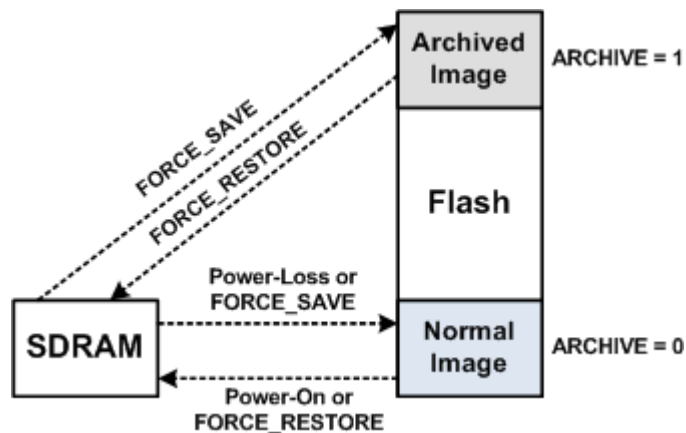


Figure 2-2 Archive Operations

The interaction varies, depending on when the signals are asserted and which operation is underway at the time:

- If the Host asserts FORCE_SAVE or FORCE_RESTORE and—while the operation is in progress—the power fails, then (POWER_FAIL_INT# asserts):
 - a. Any FORCE_RESTORE (Normal or Archive) is aborted. This is harmless, since a partially-restored SDRAM is useless if the Host loses power. At the next power-up, the SDRAM contents are correctly restored from the normal space.
 - b. A FORCE_SAVE (Normal) operation continues to completion.
 - c. A FORCE_SAVE (Archive) continues to completion, and the SDRAM data is saved to both the normal and archive areas. At the next power-on, the Normal data is automatically restored, and the Archive is kept until the next FORCE_SAVE (Archive) occurs. To separate them, the Host must do another FORCE_SAVE (Archive) operation.
- If power fails, and then power is restored during the Save operation, Bali terminates the Save operation and asserts the SYSTEM_READY signal shortly after power is good. Since a Restore operation is not necessary, this shortens the “ready-to-use” time. The SDRAM contents are still valid because Bali maintained SDRAM power during the black-out.

As noted in the section [SYSTEM_READY on page 2-14](#), the Host uses the FORCE_SAVE or FORCE_RESTORE signals, it must first prepare the SDRAM before asserting these signals as shown in the POWER_FAIL_INT# section, specifically:

1. Program the SDRAM for CL=2, BL=1, 2, or 4 if necessary.
2. Put the SDRAM into the self-refresh state.

2.5 SDRAM Information

Bali uses different types of SDRAM, depending on the Bali part number, listed in [Table 2-5](#).

Table 2-5 SDRAM Types

Bali P/N	SDRAM P/N (Micron)	SDRAM Size (MBytes)	Non-Volatile Size (MBytes)	Notes
AGIGA8003-004ACA	MT48LC16M16A2P-75	32	4	1, 2
AGIGA8004-008ACA		32	8	
AGIGA8005-016ACA		32	16	
AGIGA8006-032ACA		32	32	
AGIGA8007-064ACA	MT48LC32M16A2P-75	64	64	3, 4

NOTES:

1. SDRAM is organized as 16Mx16.
2. Vcc is 3.3V, SDRAM interface is 3.3V.
3. SDRAM is organized as 32Mx16.
4. Vcc is 5.0V, SDRAM interface is 3.3V.

The Non-Volatile size is the portion of the SDRAM that is saved to and restored from non-volatile memory, as shown in [Figure 2-3](#).

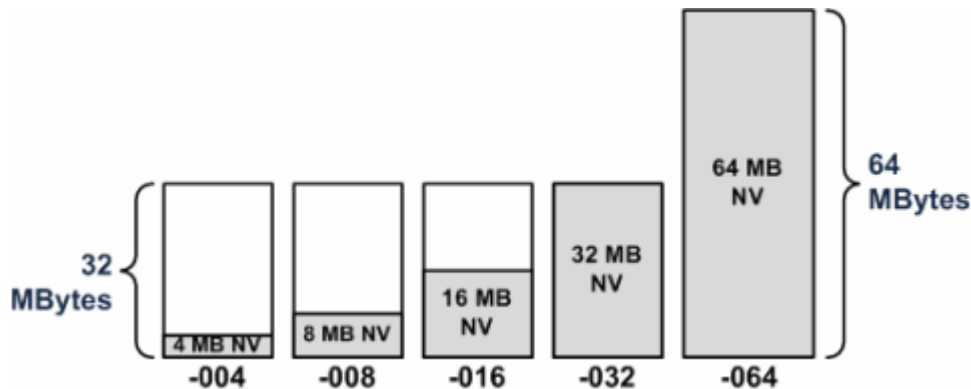


Figure 2-3 Non-Volatile Portion of SDRAM

Consult the appropriate SDRAM datasheet for information about detailed timing and functional operations. The following specifications for the Bali Non-Volatile System override those listed in the Micron SDRAM datasheet:

Table 2-6 Bali Specifications Override Micron

Feature	Bali Specification
Clock frequency	100 MHz maximum
CAS Latency	CL=2 only
Burst Length	BL=1, 2, or 4
Self-Refresh	Standard only (not Low Power)
AC Characteristics	Internal address/data/clock go through high-speed MUX which adds 0.2 ns (max) to prop delays.
Capacitance (pF)	All pins: 16 Typ, 24 Maximum

2.5.1 SDRAM Connection

Although the Bali on-board SDRAM provides a 16-bit data bus, it is internally configured for use in 32-bit systems. Therefore, Host addressing should start with A2 instead of A0, as shown in [Figure 2-4](#).

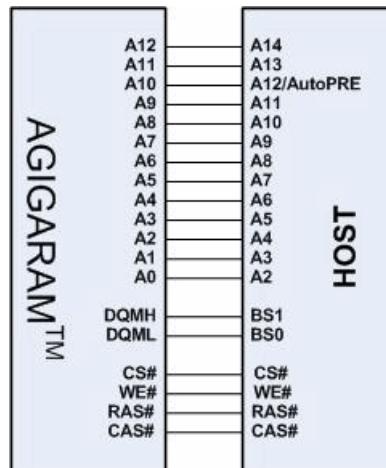


Figure 2-4 NVS-to-Host Pins

In 32-bit systems, the low address bits A0 and A1 are replaced by four Byte Select (BS) signals. This allows the CPU to retrieve words (all four BS signals active), half-words (two BS signals active), or bytes (one BS signal active).

If one Bali is used, a word (32-bit) access reads and writes data in the lower 16-bits only. If 32-bit access is required, a second Bali can be connected as shown by the dotted lines in [Figure 2-5](#).

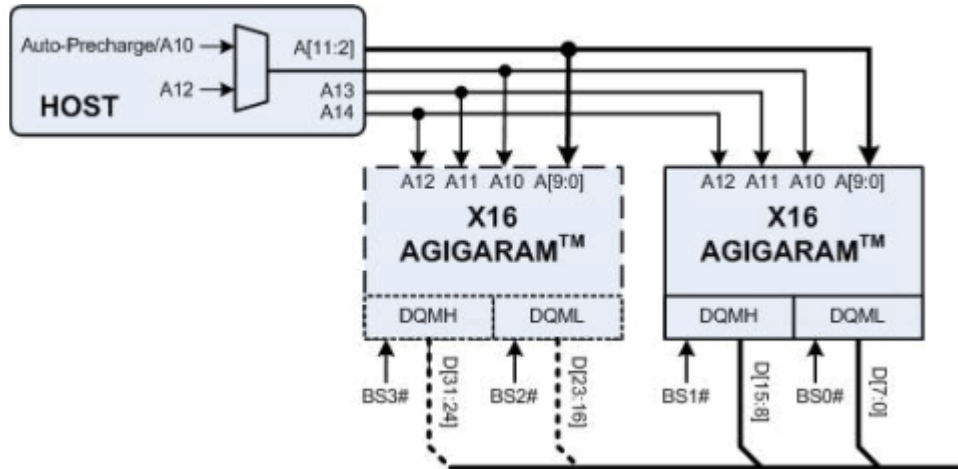


Figure 2-5 Using Two Bali Units

Although RAM address lines may usually be connected in any order, SDRAMs have a unique requirement for the A10 pin. The SDRAM controller sends a command for an auto-precharge operation by using the normal command bus (CS#, RAS#, CAS#, and WE#) *plus* the A10 signal. This is the only SDRAM command that uses an address line in addition to the command bus.

SDRAM controllers differ in how this is documented. For example, Atmel ARM processors have a second A10 signal called “SDA10”. The “SD” prefix is a reminder that this is an SDRAM signal, and it must be physically connected to the SDRAM A10 pin. The other Atmel A10 pin can be connected to any address line (for example, to pin A8, as shown earlier in [Figure 2-4](#)). In this example, the SDRAM controller multiplexes A12 with the auto-precharge signal, and the SDRAM controller signal labeled “A12” is not connected.

2.6 Bali I²C Interface

An I²C interface is available on all versions of the Bali systems.

Bali is an I²C slave with addresses 0x28 (Write) and 0x29 (Read). The I²C interface operates with serial clock (SCL) up to 400 KHz. Using this interface, the Host can replace the functions of five Bali pins with the two I²C signals SCL and SDA. If an I²C interface is used, the replaced input signals must be strapped to their inactive states as shown in [Table 2-7](#).

Table 2-7 Strapping I²C Signals

Signal	Strap Pin
FORCE_SAVE	GND
FORCE_RESTORE	GND
ARCHIVE	GND

Bali uses the following I²C commands:

- I²C Write
- I²C Read

2.6.1 I²C Write

[Figure 2-6](#) shows the format of the I²C Write command, which replaces three input pin functions.

2.6.2 I²C Read

Figure 2-7 shows the format of the I²C read command, which duplicates the states of the Bali status pins.

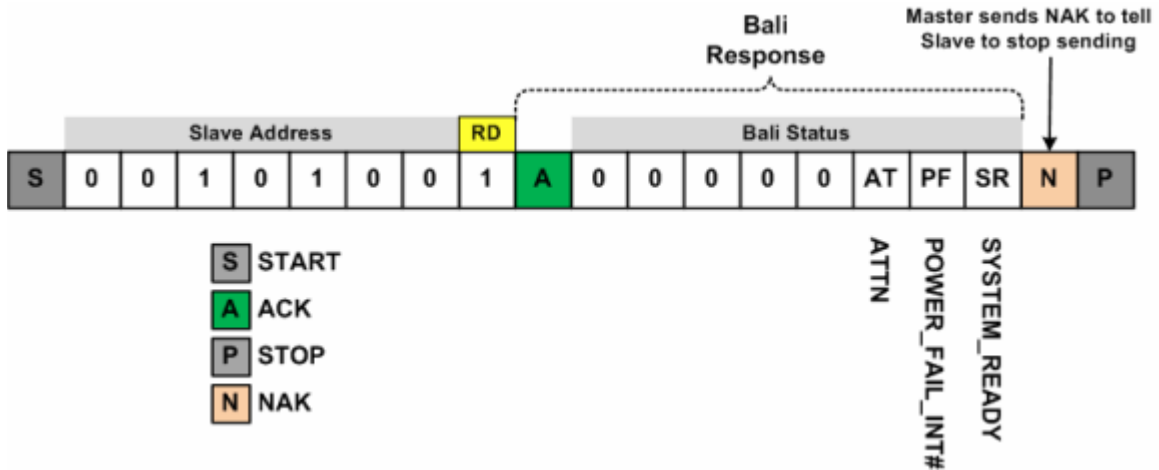


Figure 2-7 I²C Read Command

The two Bali output signals POWER_FAIL_INT# and SYSTEM_READY function identically to the descriptions shown in Table 2-4 on page 2-12. The ATTN bit reads 0, with non-zero conditions TBD. The remaining bits read as zero.

2.6.3 Using I²C to Read Temperature History

Bali keeps a record of module temperature over time that can be read by an I²C master. Two transfer types are defined for this operation:

- Read number of stored temperatures (32-bit)
- Read one temperature value (8-bit signed byte)

2.6.3.1 Read Number of Stored Temperature Values (0x93)

Bali records temperature values once per hour under 50°C and six per hour over 50°C. Figure 2-8 shows the I²C format used to retrieve the total number of temperature measurements.

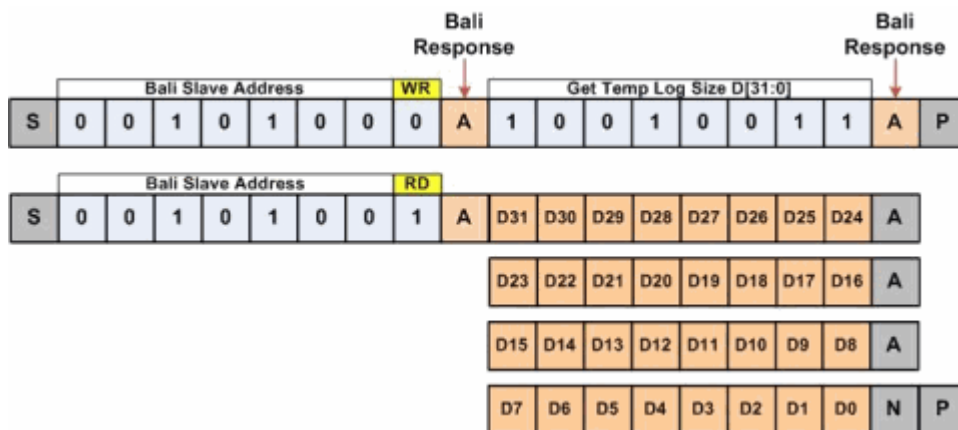


Figure 2-8 I²C Read Total Number of Stored Temperature Values

2.6.3.2 Read One Stored Temperature Value (0x94)

Temperature values are represented in °C as a signed (two’s complement) byte, giving a range of numbers, from 127°C to -128°C. [Figure 2-9](#) shows how to retrieve an individual temperature value.

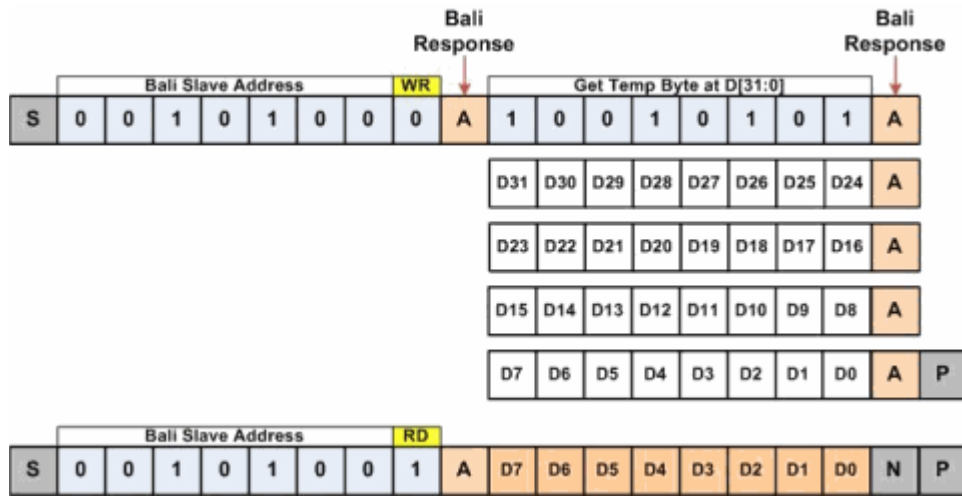


Figure 2-9 Read One Stored Temperature

[Table 2-8](#) lists the binary encoding for temperature values.

Table 2-8 Binary Values for Temperatures

D[7:0]	°C
01111111	127
01111110	126
00000010	2
00000001	1
00000000	0
11111111	-1
11111110	-2
10000001	-127
10000000	-128

2.7 LED Indicators

The Bali module has two LED indicators: one green and one red. These LEDs indicate the readiness state of the Bali module.

- The green LED indicates that the data transfer from Flash to SDRAM is in progress.
- The red LED indicates the charge state of the internal power source.

[Table 2-9](#) lists the sequence that occurs when power is applied to the module.

Table 2-9 Status of LED Indicators

Green LED	Red LED	Description
GRN=Blinking	RED=Blinking	Power is applied. Data is being restored to the SDRAM, and the power source is charging.
GRN=ON	RED=Blinking	The SDRAM contents are restored, and the power source is still charging.
GRN=ON	RED=ON	The module is ready for use. The SDRAM contents are restored and the power source is charged. At the moment in time that both lights turn on, Bali asserts the SYSTEM_READY signal.
GRN=OFF	RED=OFF	Both indicators turn off when system power is removed.

[Figure 2-10](#) shows the module with the LEDs:

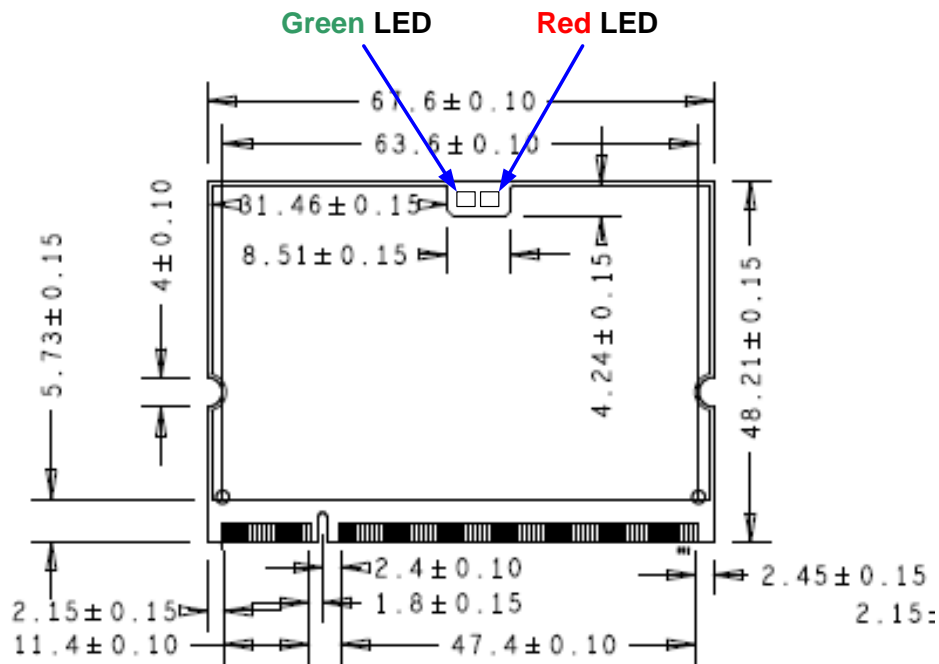



Figure 2-10 LED Locations

Electrical Specifications

This chapter describes the electrical specifications for the **AGIGARAM™** Bali Non-Volatile System.

CAUTION: ESD Sensitive Device	
	<p>Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment, and can discharge without detection. Although the system features proprietary ESD (electrostatic discharge) protection on its circuitry, permanent damage may occur on devices subjected to high energy (>250 VHBM) electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.</p>

3.1 Absolute Maximum Ratings

[Table 3-1](#) lists the absolute maximum ratings for the Bali Non-Volatile System.

Table 3-1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
3.3 V Supply Voltage	3.0	3.6	V	
5.0 V Supply Voltage	4.5	5.5	V	
Voltage on Input	-0.3	5.5	V	For Bali control signals. For SDRAM signals, consult the appropriate manufacturer's SDRAM datasheet.
Storage Temperature	-40°C	70°C	°C	

Note

Exposure to absolute maximum ratings may affect device reliability. Permanent damage may occur if the device is operated while exceeding these ratings.

3.2 AC Specifications: Control Signals

This section describes the AC specifications for the following Bali control signals:

- SYSTEM_READY
- POWER_FAIL_INT#
- FORCE_SAVE
- FORCE_RESTORE

Figure 3-1 shows the timing diagram for the SYSTEM_READY (T_{READY}) signal.

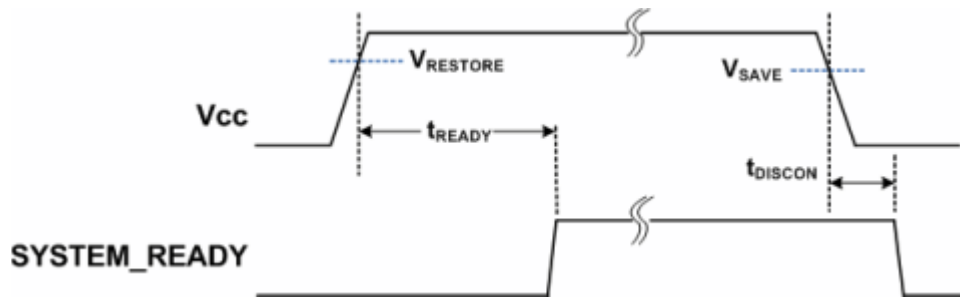


Figure 3-1 Timing for SYSTEM_READY

This figure shows the timing for SYSTEM_READY during power-on and power fail. The SDRAM is not available to the Host when SYSTEM_READY is low.

Figure 3-2 shows the timing for SYSTEM_READY for the FORCE_SAVE signal (T_{FORCE_SAVE}) signal or the FORCE_RESTORE ($T_{FORCE_RESTORE}$) signal.

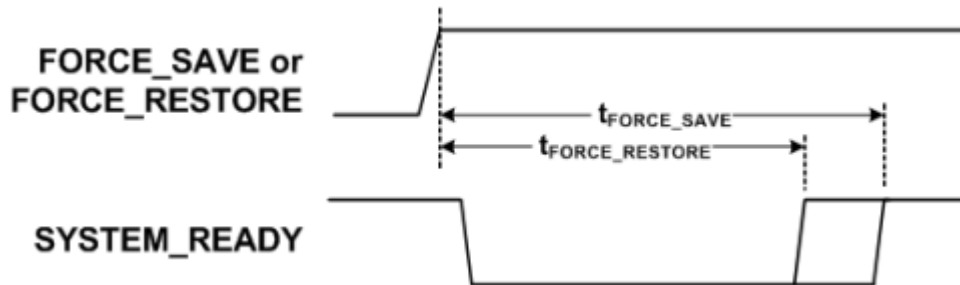


Figure 3-2 Timing for FORCE_SAVE or FORCE_RESTORE

Table 3-2 lists electrical specifications for these signals in various Bali configurations:

Table 3-2 Electrical Specifications

Bali P/N	t_{DISCON} (ms)		T_{READY} (seconds)		T_{FORCE_SAVE} (seconds)		$T_{FORCE_RESTORE}$ (seconds)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max
AGIGA8003-004ACA	1.0	1.5	4.5	5.0	0.7	0.9	0.6	0.9
AGIGA8004-008ACA	1.0	1.5	4.5	5.0	1.2	1.4	1.1	1.4
AGIGA8005-016ACA	1.0	1.5	4.5	5.0	2.3	2.6	2.0	2.3
AGIGA8006-032ACA	1.0	1.5	4.5	5.0	4.6	5.1	3.9	4.4
AGIGA8007-064ACA	1.0	1.5	8.5	9.0	8.9	9.3	8.2	8.6

3.3 DC Specifications: Control Signals

Table 3-3 lists the DC specifications for Bali control signals.

Table 3-3 DC Specifications for Control Signals

Parameter	Minimum	Typ	Maximum	Notes
SYSTEM_READY, POWER_FAIL_INT# Internal pull-up resistor to Vcc	5.5K	10K	23K	Ohms
FORCE_SAVE, FORCE_RESTORE, and ARCHIVE Internal pull-down resistor to GND	90K	100K	110K	Ohms

3.4 Power Consumption

Bali is powered by a single V_{CC} supply, which can be 3.3V or 5.0V. I_{CC} varies with system operation. [Table 3-4](#) lists the power consumption for both power supplies.

Table 3-4 Power Consumption

Condition	I_{CC} (Maximum)
Power On until T_{READY}	1.5 A
After T_{READY}	100 mA

3.5 Operating Frequencies

[Table 3-5](#) lists the operating frequencies for Bali Non-Volatile Systems.

Table 3-5 Operating Frequencies

Parameter	@CL2
Maximum Clock Frequency	100 MHz (10ns)
CL- T_{RCD} - T_{RP} (Clock)	2-2-2

3.6 Threshold Values

[Table 3-6](#) lists the threshold values for the V_{SAVE} and $V_{RESTORE}$ parameters.

Table 3-6 Threshold Values

Parameter	3.3V System	5.0V System
$V_{RESTORE}$	2.9 V	4.4 V
V_{SAVE}	2.6 V	4.0 V

This chapter describes packaging used for the **AGIGARAM™** Bali Non-Volatile System.

4.1 Package Views

The Bali Non-Volatile System is packaged in a 200-pin package.

Note

Although the Bali package fits into the same connector as a 200-pin SOIMM, it is **not** pin-compatible with SDRAM modules that use this connector.

This package can be ordered only as a lead (Pb)-free, RoHS-compliant module.

The top view is shown in [Figure 4-1](#).

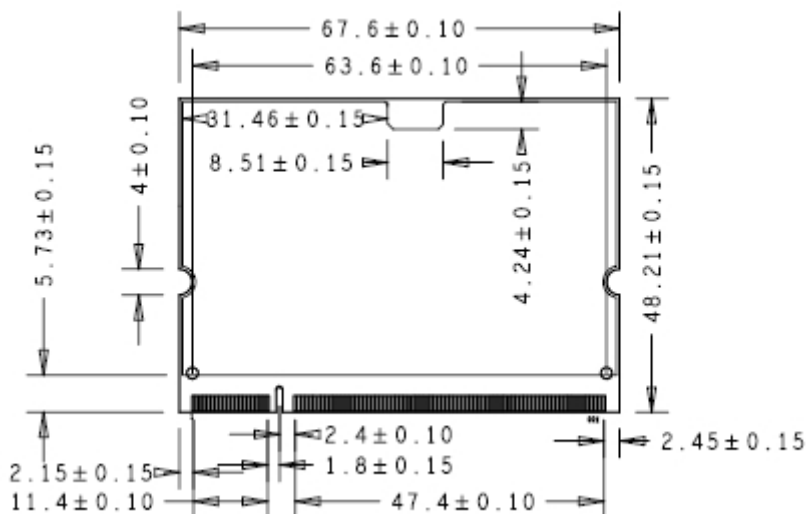


Figure 4-1 Top View

The bottom view is shown in [Figure 4-2](#):

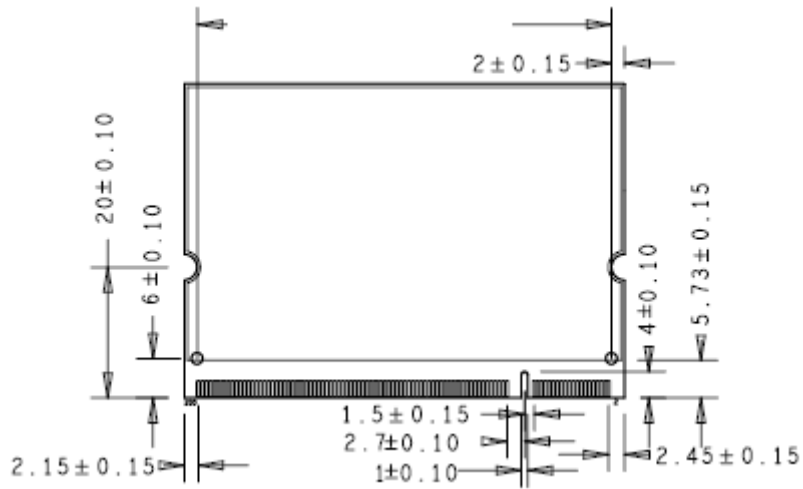


Figure 4-2 Bottom View

The side view in [Figure 4-3](#) shows the thickness of the module:

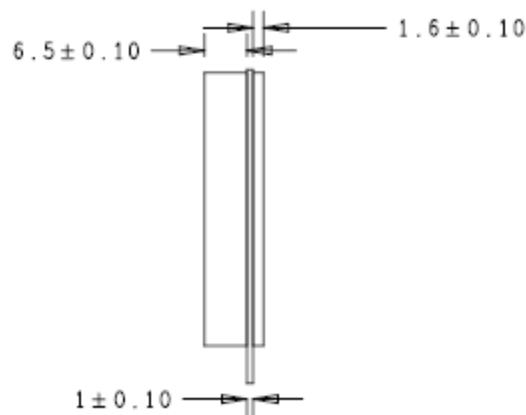


Figure 4-3 Side View